



SINGLE M-LVDS RECEIVERS

FEATURES

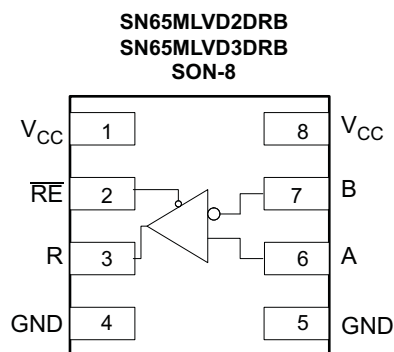
- Low-Voltage Differential 30-Ω to 55-Ω Line Receivers for Signaling Rates⁽¹⁾ up to 250Mbps; Clock Frequencies up to 125MHz
- SN65MLVD2 Type-1 Receiver Incorporates 25 mV of Input Threshold Hysteresis
- SN65MLVD3 Type-2 Receiver Provides 100 mV Offset Threshold to Detect Open-Circuit and Idle-Bus Conditions
- Wide Receiver Input Common-Mode Voltage Range, -1 V to 3.4 V, Allows 2 V of Ground Noise
- Improved V_{IT} (35 mV)
- Meets or Exceeds the M-LVDS Standard TIA/EIA-899 for Multipoint Topology
- High Input Impedance with Low Supply Voltage
- Bus-Pin HBM ESD Protection Exceeds 9 kV
- Packaged in 8-Pin SON (DRB) 70% Smaller Than 8-Pin SOIC

⁽¹⁾ The signaling rate of a line is the number of voltage transitions that are made per second, expressed in the units bps (bits per second).

APPLICATIONS

- Parallel Multipoint Data and Clock Transmission via Backplanes and Cables
- Cellular Base Stations
- Central Office Switches
- Network Switches and Routers

PACKAGE AND PIN-OUT



DESCRIPTION

The SN65MLVD2 and SN65MLVD3 are single-channel M-LVDS receivers. These devices are designed in full compliance with the TIA/EIA-899 (M-LVDS) standard, which are optimized to operate at signaling rates up to 250 Mbps. Each receiver channel is controlled by a receive enable (\overline{RE}). When \overline{RE} = low, the corresponding channel is enabled; when \overline{RE} = high, the corresponding channel is disabled.

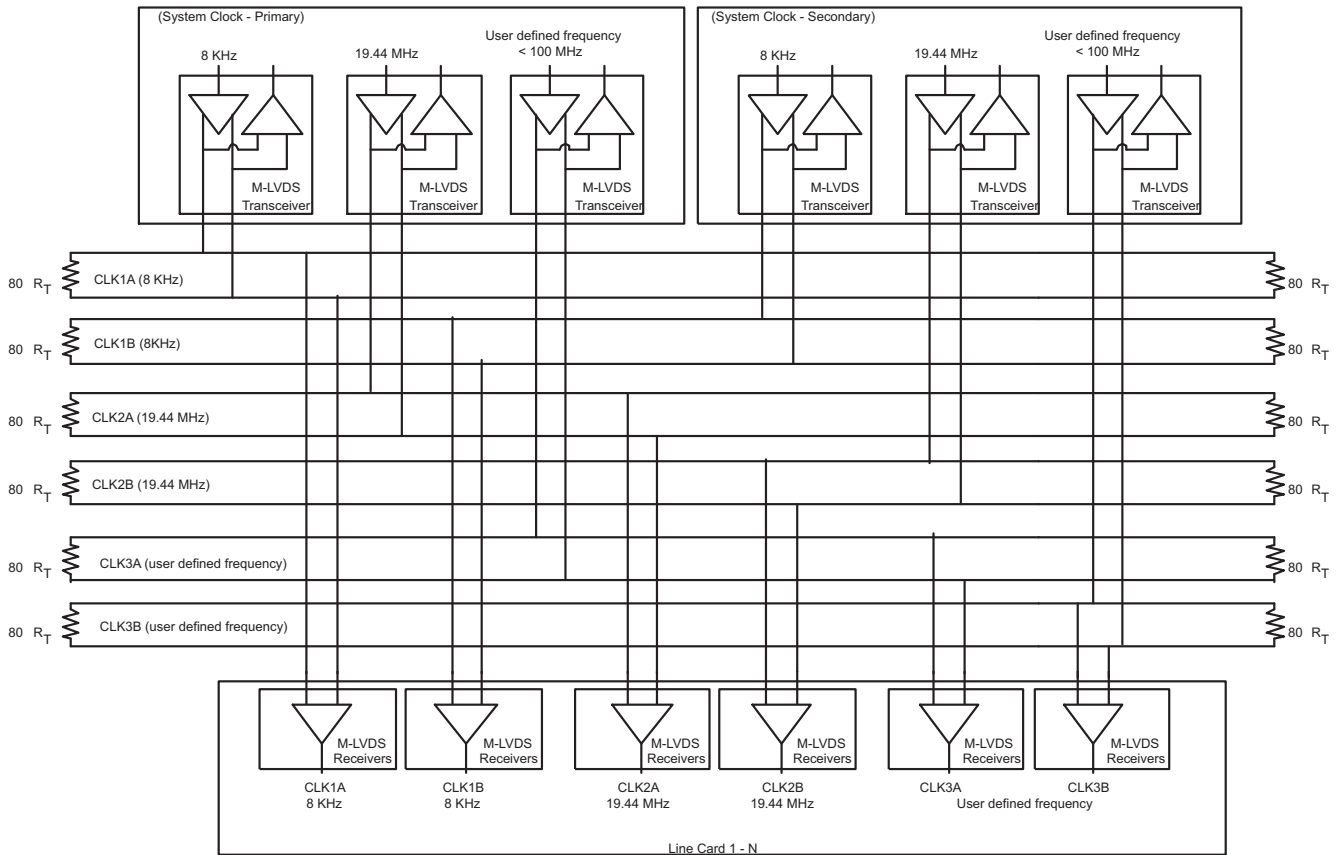
The M-LVDS standard defines two types of receivers, designated as Type-1 and Type-2. Type-1 receivers (SN65MLVD2) have thresholds centered about zero with 25 mV of hysteresis to prevent output oscillations with loss of input; Type-2 receivers (SN65MLVD3) implement a failsafe by using an offset threshold. Receiver outputs are slew rate controlled to reduce EMI and crosstalk effects associated with large current surges.

The devices are characterized for operation from -40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TYPICAL APPLICATION



AdvancedTCA Backplane - Synchronized System Clock



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION⁽¹⁾

PART NUMBER	FUNCTION	PART MARKING	PACKAGE / CARRIER
SN65MLVD2DRBT	M-LVDS Type 1 Receiver	MF2	8-Pin SON / Small Tape and Reel
SN65MLVD2DRBR	M-LVDS Type 1 Receiver	MF2	8-Pin SON / Tape and Reel
SN65MLVD3DRBT	M-LVDS Type 2 Receiver	MF3	8-Pin SON / Small Tape and Reel
SN65MLVD3DRBR	M-LVDS Type 2 Receiver	MF3	8-Pin SON / Tape and Reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		VALUE	UNIT	
V_{CC}	Supply voltage range ⁽²⁾	–0.5 to 4	V	
Input voltage range	RE	–0.5 to 4	V	
	A or B	–1.8 to 4	V	
Output voltage range	R	–0.3 to 4	V	
Electrostatic discharge	Human-body model ⁽³⁾	All other pins	±7	kV
		A, B	±9	
	Machine model ⁽⁴⁾	All pins	±200	V
	Field-induced-charged-device model ⁽⁵⁾	All pins	±2	kV
Continuous power dissipation		See Dissipation Rating Table		

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-A. Bus pin stressed with respect to a common connection of GND and V_{CC} .
- (4) Tested in accordance with JEDEC Standard 22 Test Method A115-A.
- (5) Tested in accordance with EIA-JEDEC JESD22-C101C.

PACKAGE DISSIPATION RATINGS⁽¹⁾

PACKAGE	PCB TYPE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ⁽²⁾ ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
8-SON DRB	Low-K	280 mW	2.80 mW/°C	112 mW
	High-K	662 mW	6.62 mW/°C	264 mW

- (1) The thermal dissipations are in the consideration of soldering down the powerPAD without via on each type of boards.
- (2) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

THERMAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JB} Junction-to-board thermal resistance			89		°C/W
θ_{JC} Junction-to-case thermal resistance			98		°C/W
P_D Device power dissipation	RE at 0 V, $C_L = 15$ pF, $V_{ID} = 400$ mV, 125 MHz			90	mW

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	GND		0.8	V
V_A or V_B	Voltage at any bus terminal	-1.4		3.8	V
$ V_{ID} $	Magnitude of differential input voltage	0.035		V_{CC}	V
V_{IC}	Differential common-mode input voltage	-1		3.4	V
R_L	Differential load resistance	30	50		Ω
$1/t_{UI}$	Signaling rate			250	Mbps
T_A	Operating free-air temperature	-40		85	$^{\circ}\text{C}$

DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT	
I_{CC}	Supply current	\overline{RE} at 0 V, $C_L = 15$ pF, $V_{ID} = 400$ mV, 125 MHz			25	mA

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold	Type 1		35	mV
		Type 2		135	
V_{IT-}	Negative-going differential input voltage threshold	Type 1		-35	mV
		Type 2		65	
V_{HYS}	Differential input voltage hysteresis ($V_{IT+} - V_{IT-}$)	Type 1		25	mV
		Type 2		0	
V_{OH}	High-level output voltage	$I_{OH} = -8$ mA			V
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA			V
I_{IH}	High-level input current	$V_{IH} = 2$ V to V_{CC}			μA
I_{IL}	Low-level input current	$V_{IL} = \text{GND}$ to 0.8 V			μA
I_{OZ}	High-impedance output current	$V_O = 0$ V or V_{CC}			μA
I_A or I_B	Receiver input current	One input (V_A or V_B) = -1.4 V or 3.8 V, Other input = 1.2 V			μA
I_{AB}	Receiver differential input current ($I_A - I_B$)	$V_A = V_B = -1.4$ V or 3.8 V			μA
$I_{A(OFF)}$ or $I_{B(OFF)}$	Receiver input current	One input (V_A or V_B) = -1.4 V or 3.8 V, Other input = 1.2 V, $V_{CC} = \text{GND}$ or 1.5 V			μA
$I_{AB(OFF)}$	Receiver power-off differential input current ($I_A - I_B$)	$V_A = V_B = -1.4$ V or 3.8 V, $V_{CC} = \text{GND}$ or 1.5 V			μA
C_A or C_B	Input capacitance	$V_I = 0.4\sin(30E6\pi t) + 0.5\text{V}$, ⁽²⁾ Other input at 1.2 V			pF
C_{AB}	Differential input capacitance	$V_{AB} = 0.4\sin(30E6\pi t) + 0.5\text{V}$ ⁽²⁾			pF
$C_{A/B}$	Input capacitance balance, (C_A/C_B)	0.99		1.01	

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

(2) HP4194A impedance analyzer (or equivalent)

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT	
t _{PLH}	Propagation delay time, low-to-high-level output	C _L = 15 pF, See Figure 2	2		6	ns	
t _{PHL}	Propagation delay time, high-to-low-level output		2		6	ns	
t _r	Output signal rise time		1		2.3		
t _f	Output signal fall time		1		2.3	ns	
t _{sk(p)}	Pulse skew (t _{PHL} – t _{PLH})		Type 1		90	210	ps
			Type 2		45	250	
t _{sk(pp)}	Part-to-part skew				1	ns	
t _{jit(per)}	Period jitter, rms (1 standard deviation) ⁽²⁾		125 MHz clock input			10	ps
t _{jit(c-c)}	Cycle-to-cycle jitter, rms ⁽³⁾		125 MHz clock input ⁽⁴⁾			8	ps
t _{jit(det)}	Deterministic jitter ⁽²⁾		Type 1	250 Mbps 2 ¹⁵ -1 PRBS input ⁽⁵⁾		500	ps
		Type 2			450	ps	
t _{jit(ran)}	Random jitter ⁽²⁾	Type 1	250 Mbps 2 ¹⁵ -1 PRBS input ⁽⁵⁾		8	ps	
		Type 2			8	ps	
t _{PZH}	Enable time, high-impedance-to-high-level output	C _L = 15 pF, See Figure 3			15	ns	
t _{PZL}	Enable time, high-impedance-to-low-level output	C _L = 15 pF, See Figure 3			15	ns	
t _{PHZ}	Disable time, high-level-to-high-impedance output	C _L = 15 pF, See Figure 3			10	ns	
t _{PLZ}	Disable time, low-level-to-high-impedance output	C _L = 15 pF, See Figure 3			10	ns	

- (1) All typical values are at 25°C and with a 3.3-V supply voltage.
- (2) Jitter measured by triggering off of the input source to track out the associated input jitter.
- (3) Stimulus jitter has been subtracted from the numbers.
- (4) Measured over 75K samples
- (5) Measured over BER = 10⁻⁶.

TERMINAL FUNCTIONS

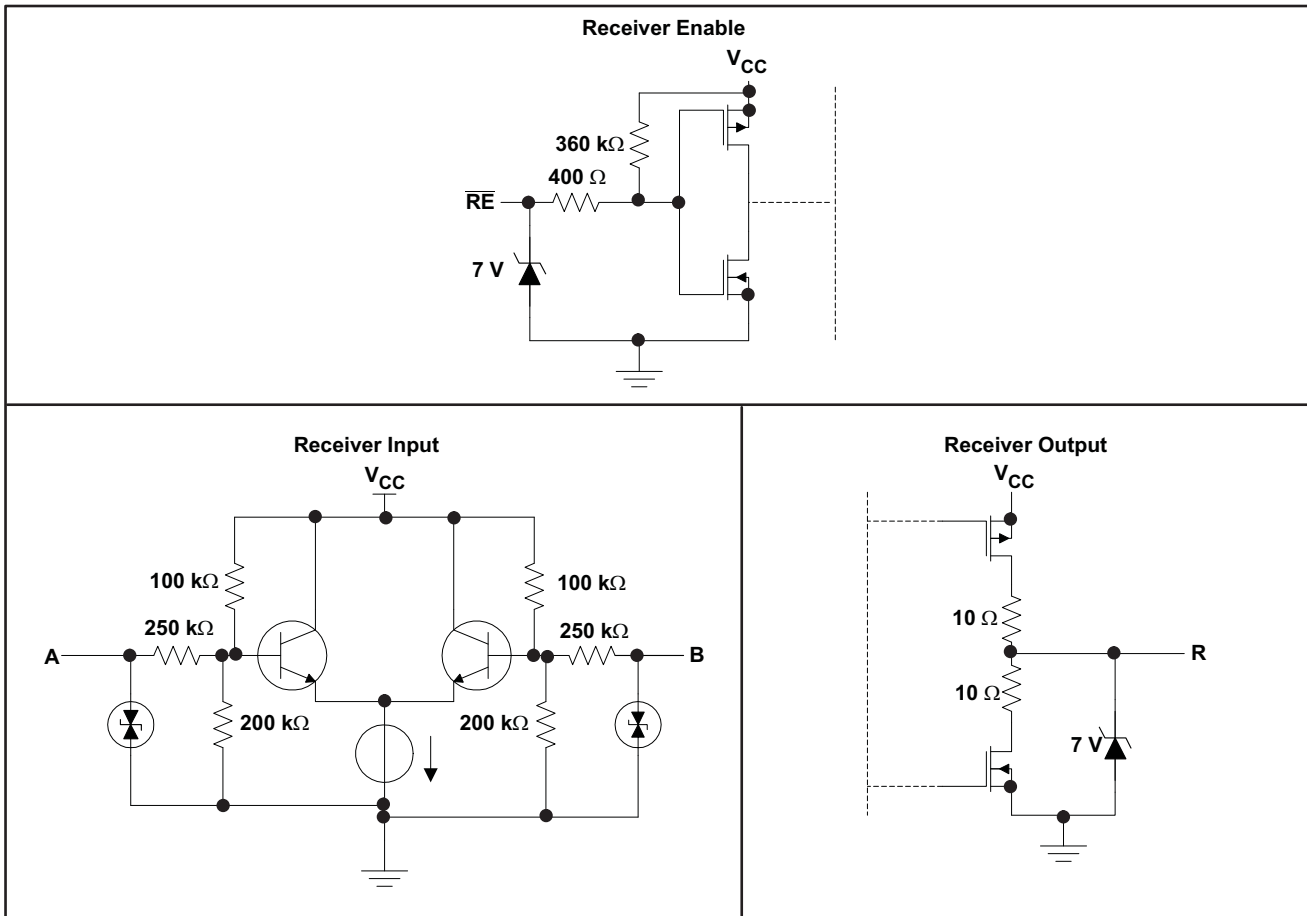
TERMINAL		I/O	DESCRIPTION
NAME	NO.		
A	6	I	M-LVDS Non-inverting input
B	7	I	M-LVDS Inverting input
R	3	O	Data output from receivers
\overline{RE}	2	I	Receiver enable, active low, enables all receivers
GND	4, 5		Circuit ground
V _{CC}	1, 8		Supply voltage

DEVICE FUNCTION TABLES

TYPE-1 RECEIVER (SN65MLVD2)			TYPE-2 RECEIVER (SN65MLVD3)		
INPUTS ⁽¹⁾		OUTPUT ⁽¹⁾	INPUTS ⁽¹⁾		OUTPUT ⁽¹⁾
V _{ID} = V _A – V _B	\overline{RE}	R	V _{ID} = V _A – V _B	\overline{RE}	R
V _{ID} ≥ 35 mV	L	H	V _{ID} ≥ 135 mV	L	H
–35 mV ≤ V _{ID} ≤ 35 mV	L	?	65 mV ≤ V _{ID} ≤ 135 mV	L	?
V _{ID} ≤ –35 mV	L	L	V _{ID} ≤ 65 mV	L	L
X	H	Z	X	H	Z
X	Open	Z	X	Open	Z
Open Circuit	L	?	Open Circuit	L	L

- (1) H=high level, L=low level, Z=high impedance, X=Don't care, ?=indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



PARAMETER MEASUREMENT INFORMATION

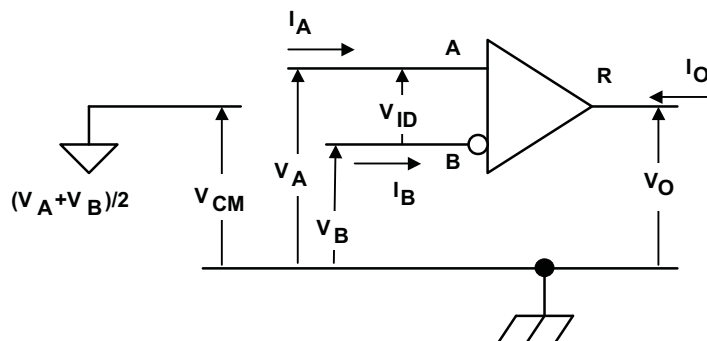


Figure 1. Receiver Voltage and Current Definitions

Table 1. Type-1 Receiver Input Threshold Test Voltages

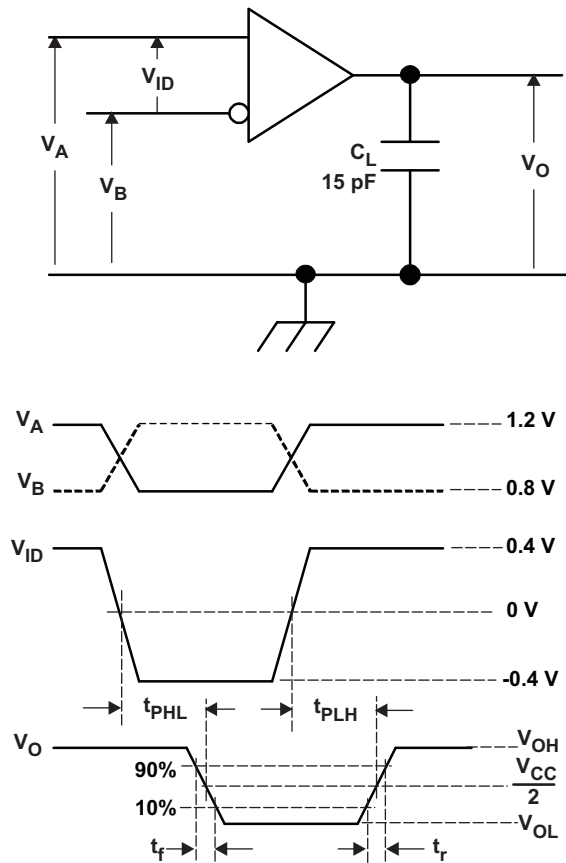
APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	RECEIVER OUTPUT ⁽¹⁾
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	-2.400	1.200	L
3.400	3.365	0.035	3.3825	H
3.365	3.400	-0.035	3.3825	L
-0.965	-1	0.035	-0.9825	H
-1	-0.965	-0.035	-0.9825	L

(1) H= high level, L = low level, output state assumes receiver is enabled ($\overline{RE} = L$)

Table 2. Type-2 Receiver Input Threshold Test Voltages

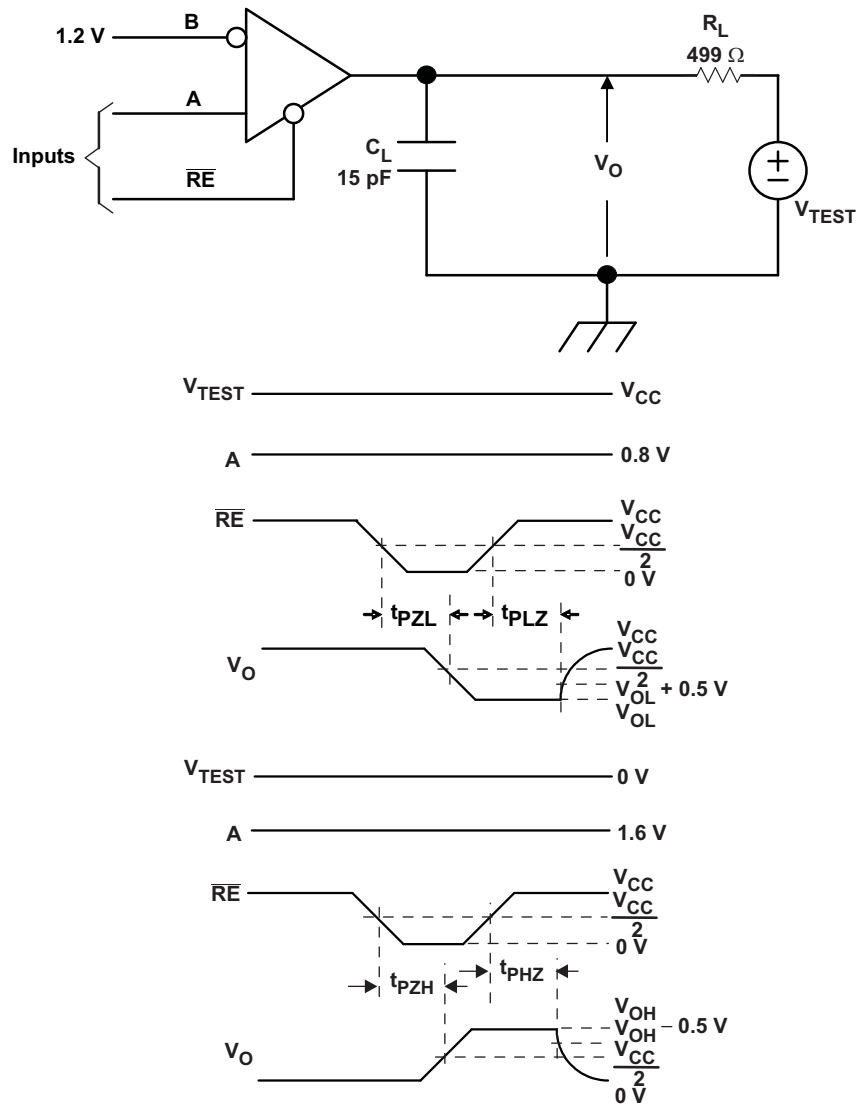
APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	RECEIVER OUTPUT ⁽¹⁾
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	-2.400	1.200	L
3.400	3.265	0.135	3.3325	H
3.4000	3.335	0.065	3.3675	L
-0.865	-1	0.135	-0.9325	H
-0.935	-1	0.065	-0.9675	L

(1) H= high level, L = low level, output state assumes receiver is enabled ($\overline{RE} = L$)



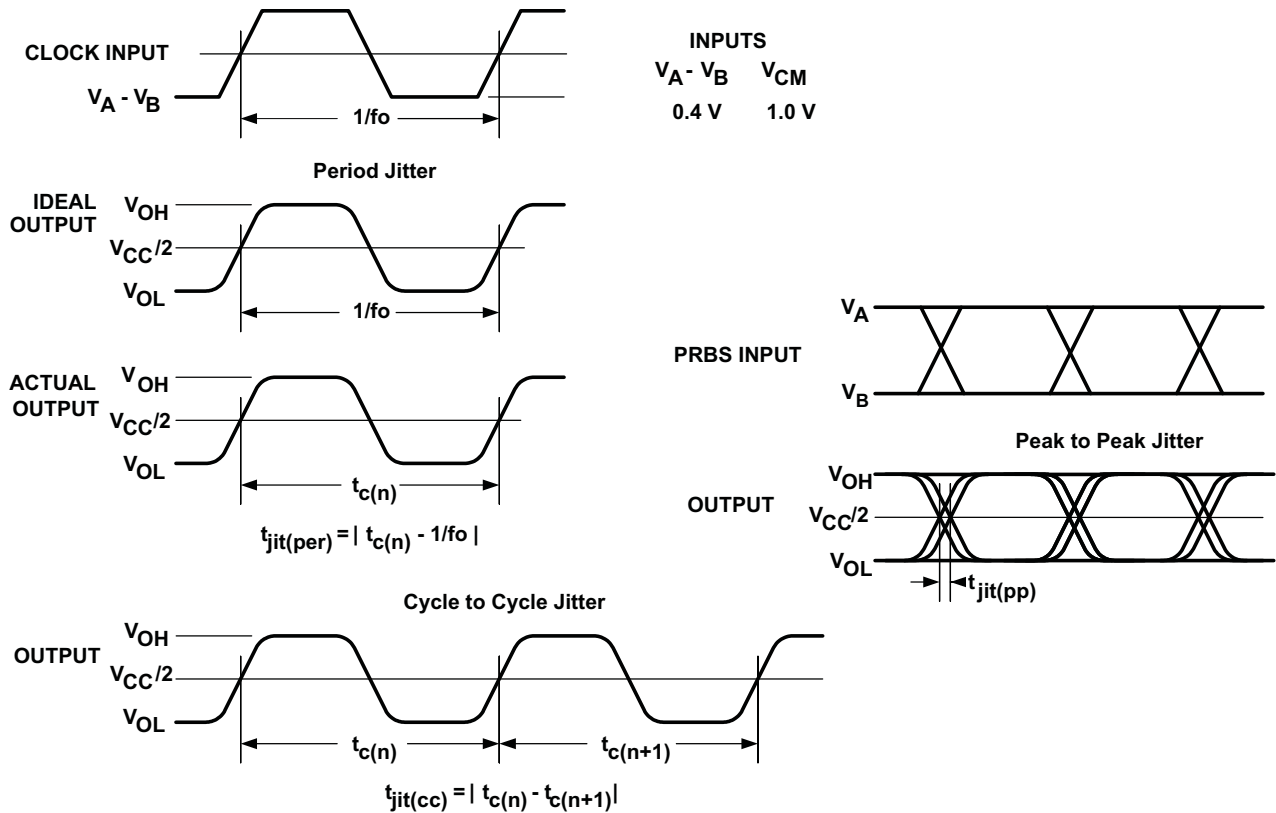
- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1 \text{ ns}$, Frequency = 1 MHz, duty cycle = $50 \pm 5\%$. C_L is a combination of a 20%-tolerance, low-loss ceramic, surface-mount capacitor and fixture capacitance within 2 cm of the D.U.T.
- B. The measurement is made on test equipment with a -3dB bandwidth of at least 1 GHz.

Figure 2. Receiver Timing Test Circuit and Waveforms



- All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, frequency = 1 MHz, duty cycle = $50 \pm 5\%$.
- R_L is 1% tolerance, metal film, surface mount, and located within 2 cm of the D.U.T
- C_L is the instrumentation and fixture capacitance within 2 cm of the D.U.T. and $\pm 20\%$. The measurement is made on test equipment with a -3dB bandwidth of at least 1GHz.

Figure 3. Receiver Enable/Disable Time Test Circuit and Waveforms



- A. All input pulses are supplied by the Agilent 81250 Parallel BERT Stimulus System with plug-in E4832A.
- B. The cycle-to-cycle jitter measurement is made on a TEK TDS6604 running TDSJIT3 application software
- C. Period jitter is measured using a 125-MHz $50 \pm 1\%$ duty cycle clock input.
- D. Deterministic jitter and random jitter are measured using a 250-Mbps 2^{15-1} PRBS input

Figure 4. Receiver Jitter Measurement Waveforms

TYPICAL CHARACTERISTICS

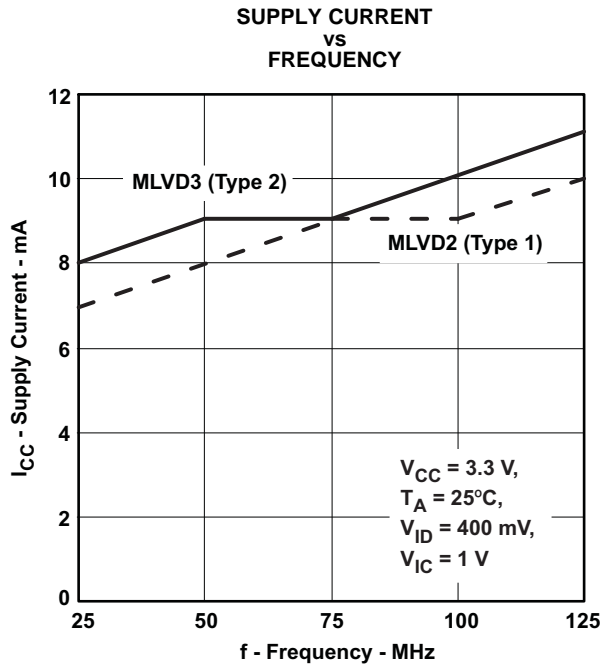


Figure 5.

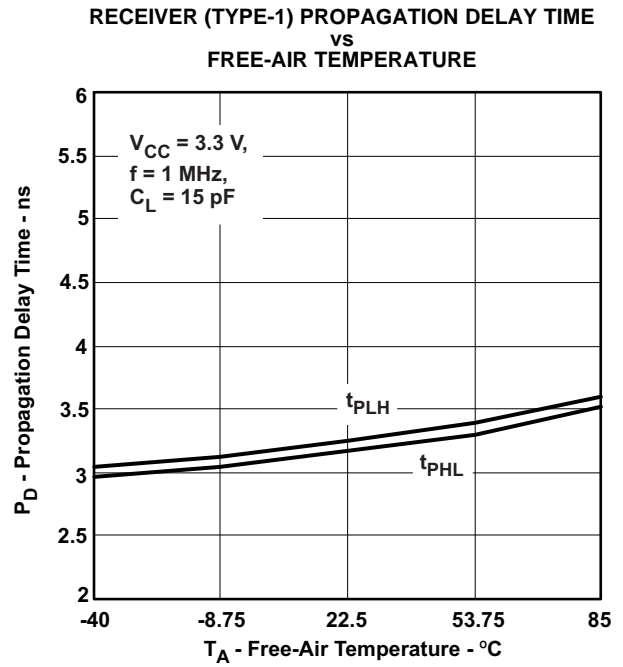


Figure 6.

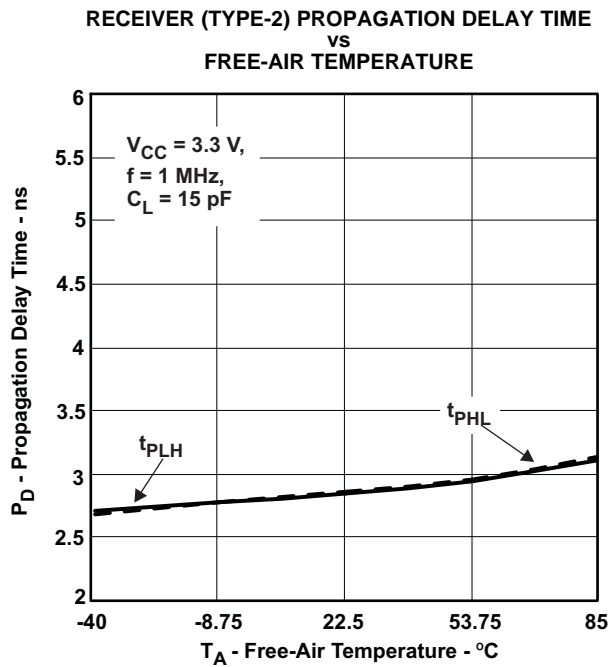


Figure 7.

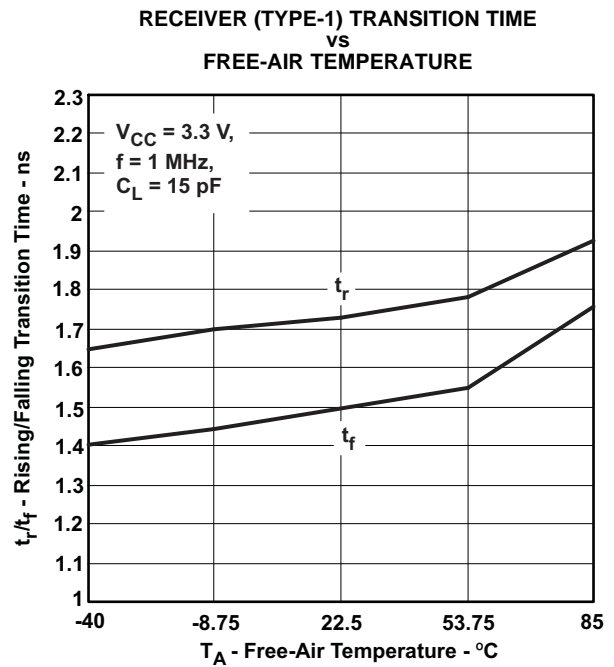


Figure 8.

TYPICAL CHARACTERISTICS (continued)

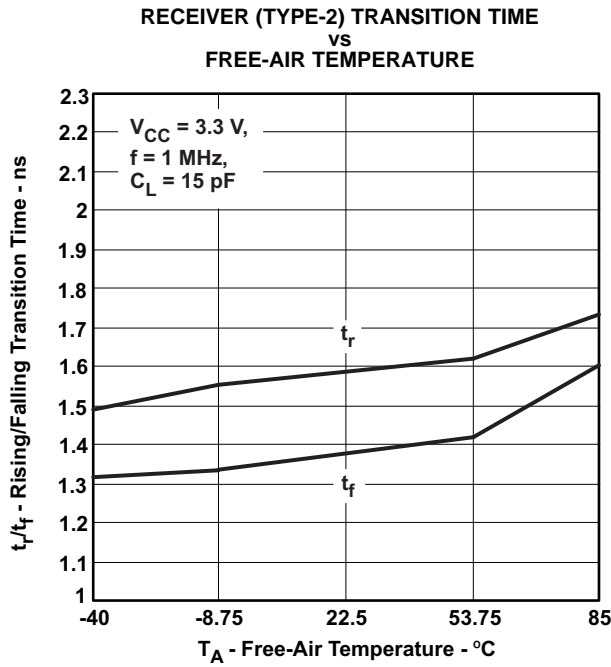


Figure 9.

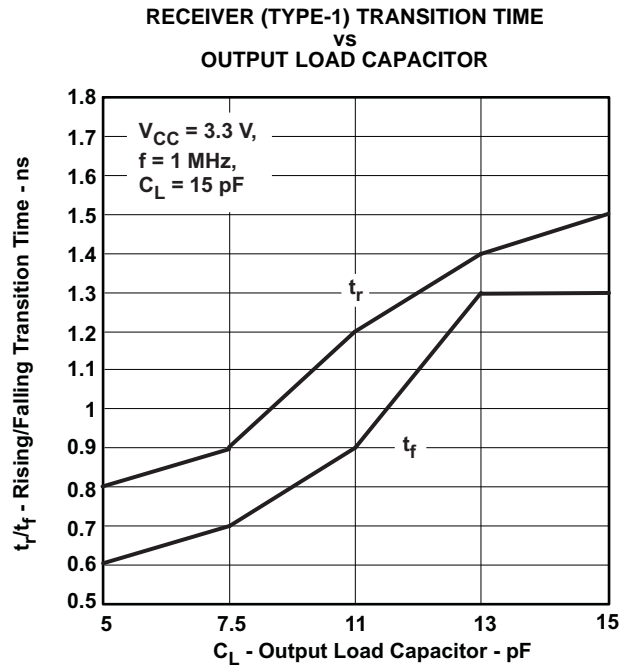


Figure 10.

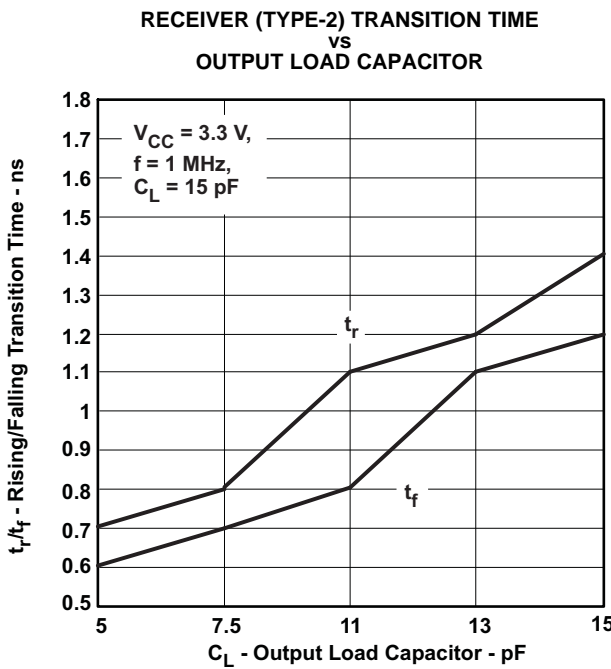


Figure 11.

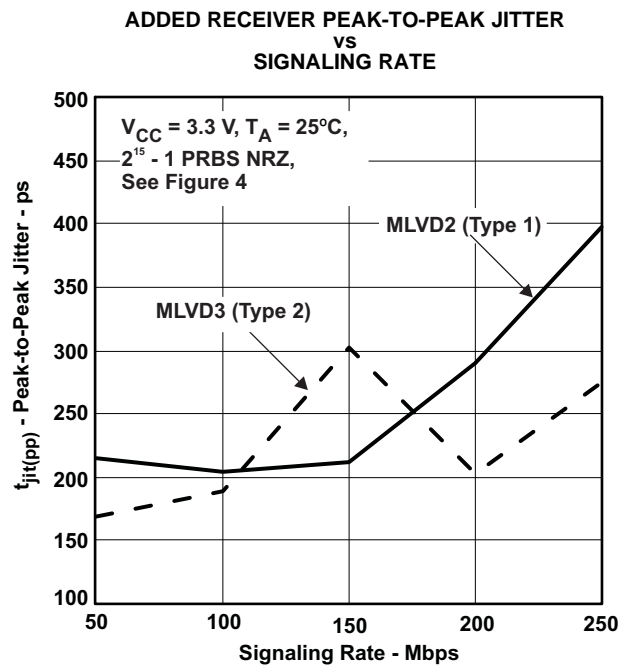


Figure 12.

TYPICAL CHARACTERISTICS (continued)

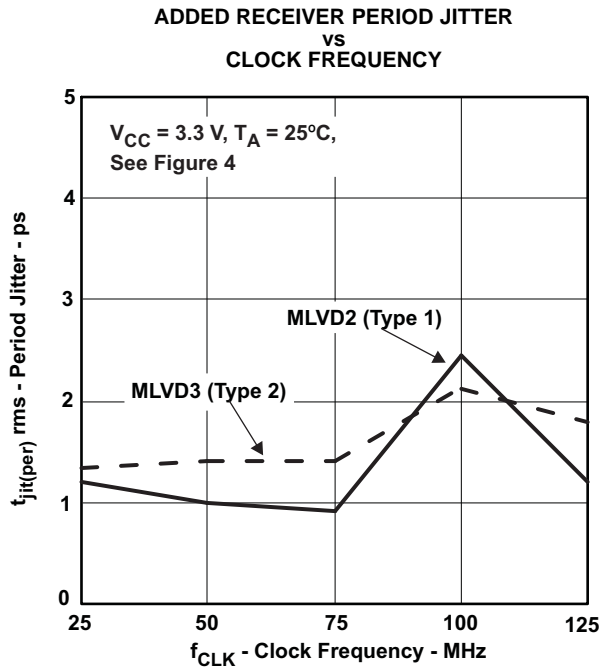


Figure 13.

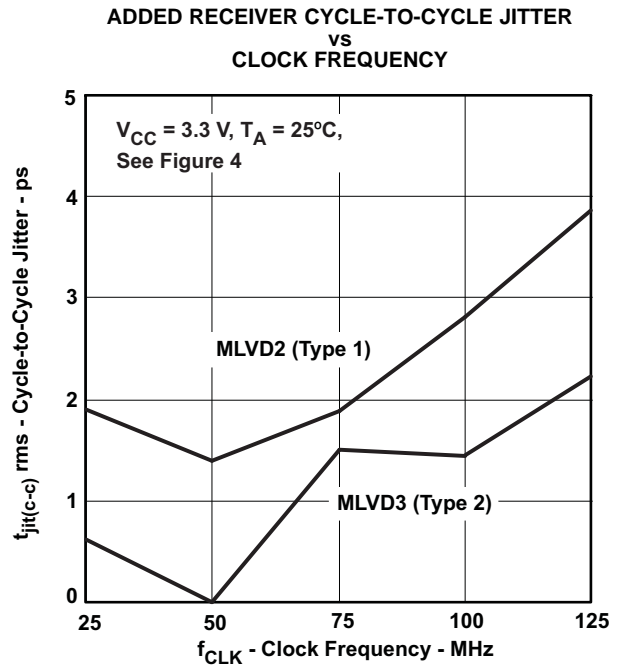


Figure 14.

EYE PATTERNS

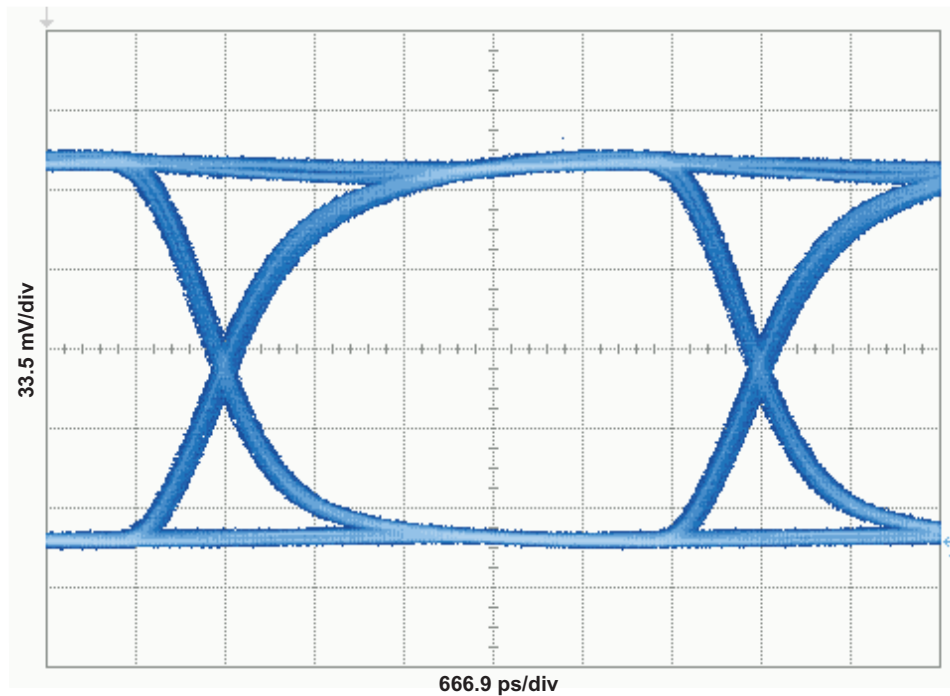


Figure 15. SN65MLVD2 Output ($V_{CC} = 3.3\text{ V}$, $C_L = 15\text{ pF}$) 250 Mbps $2^{15}-1$ PRBS

TYPICAL CHARACTERISTICS (continued)

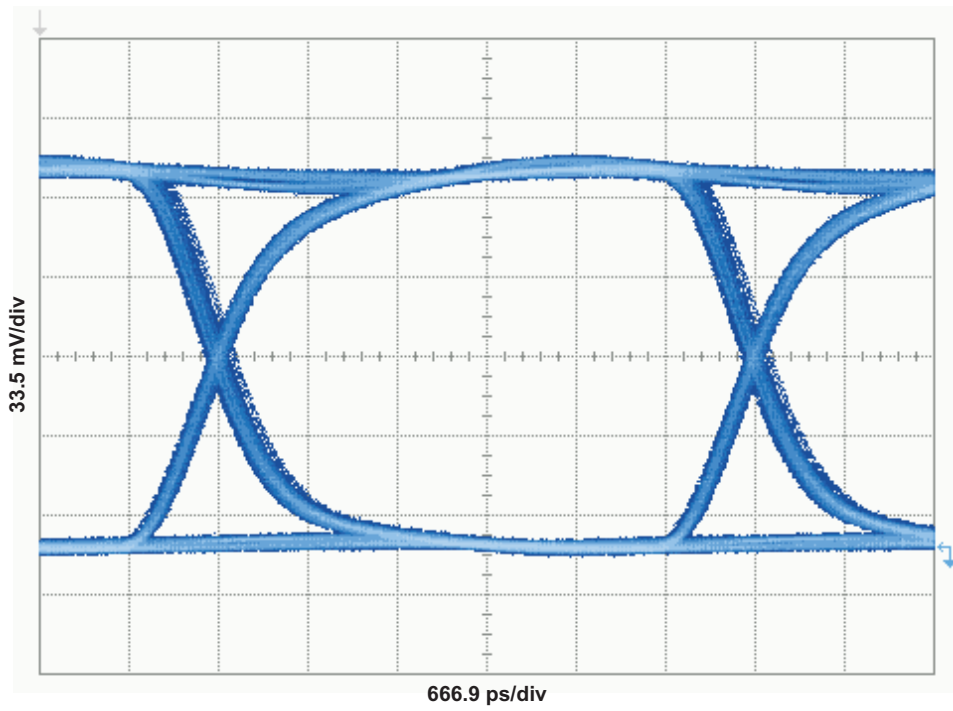


Figure 16. SN65MLVD3 Output ($V_{CC} = 3.3\text{ V}$, $C_L = 15\text{ pF}$) 250 Mbps $2^{15}-1$ PRBS

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65MLVD2DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65MLVD2DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65MLVD2DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65MLVD2DRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65MLVD3DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65MLVD3DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65MLVD3DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65MLVD3DRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

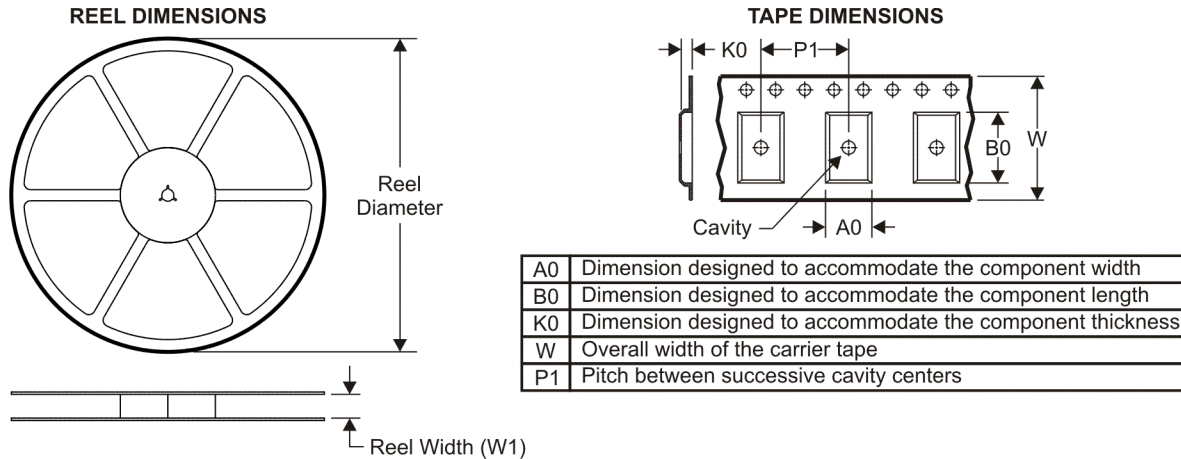
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65MLVD2DRBR	SON	DRB	8	3000	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
SN65MLVD2DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
SN65MLVD3DRBR	SON	DRB	8	3000	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
SN65MLVD3DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

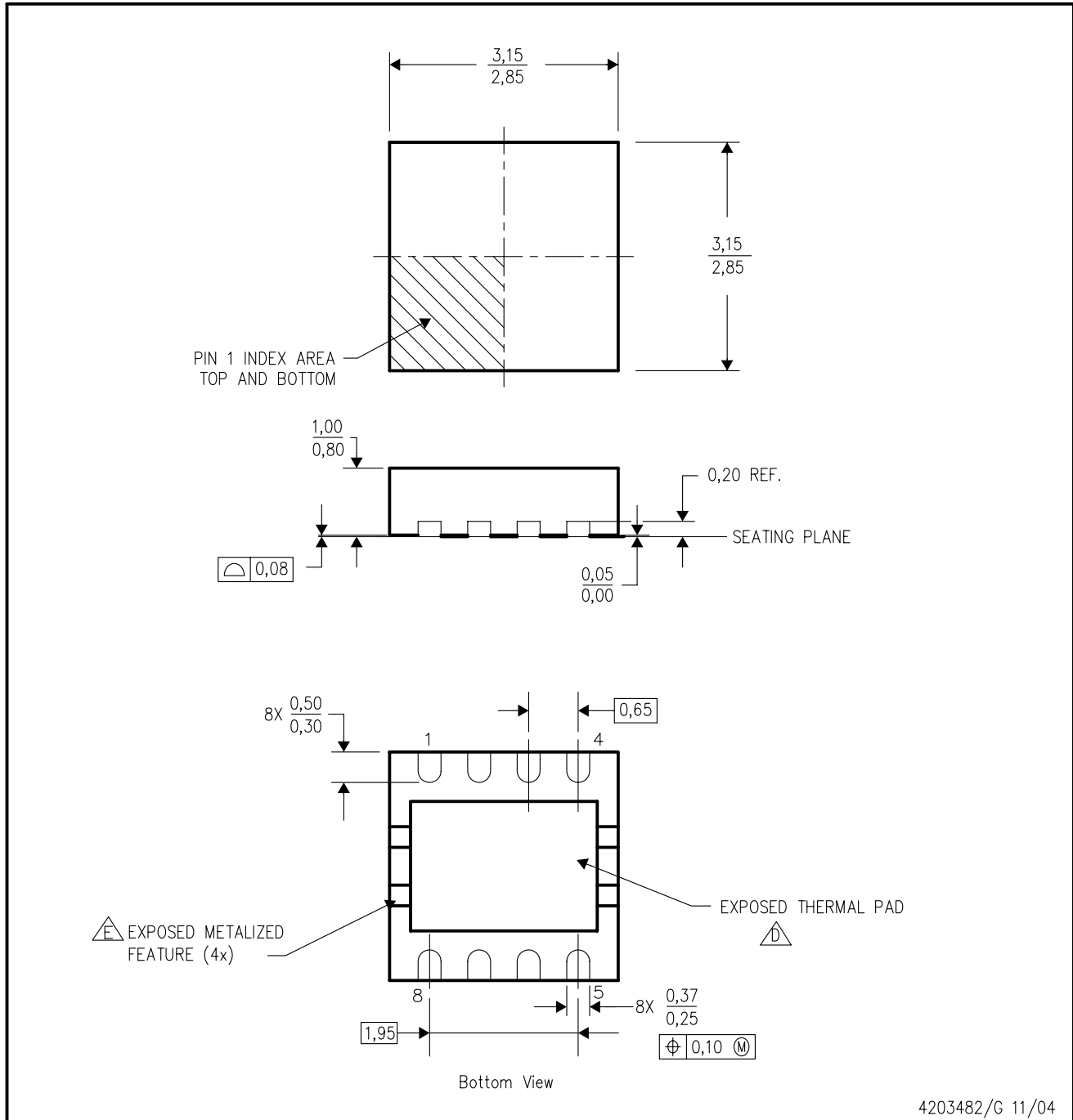




*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65MLVD2DRBR	SON	DRB	8	3000	346.0	346.0	29.0
SN65MLVD2DRBT	SON	DRB	8	250	190.5	212.7	31.8
SN65MLVD3DRBR	SON	DRB	8	3000	346.0	346.0	29.0
SN65MLVD3DRBT	SON	DRB	8	250	190.5	212.7	31.8

DRB (S-PDSO-N8)

PLASTIC SMALL OUTLINE



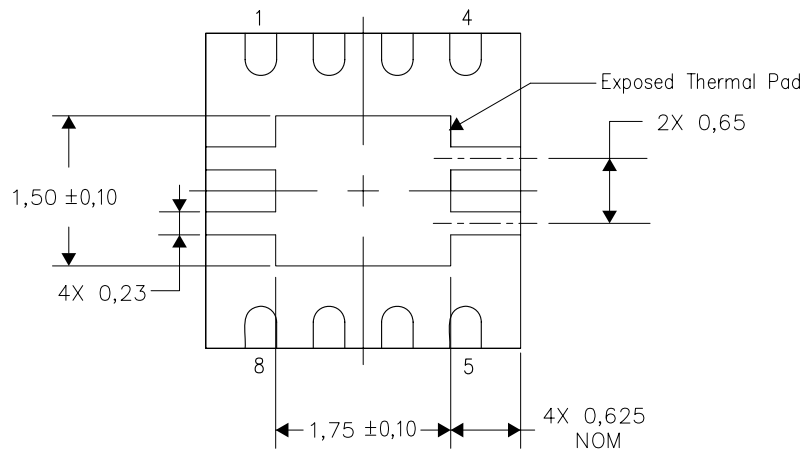
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Small Outline No-Lead (SON) package configuration.
 -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 -  Metalized features are supplier options and may not be on the package.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

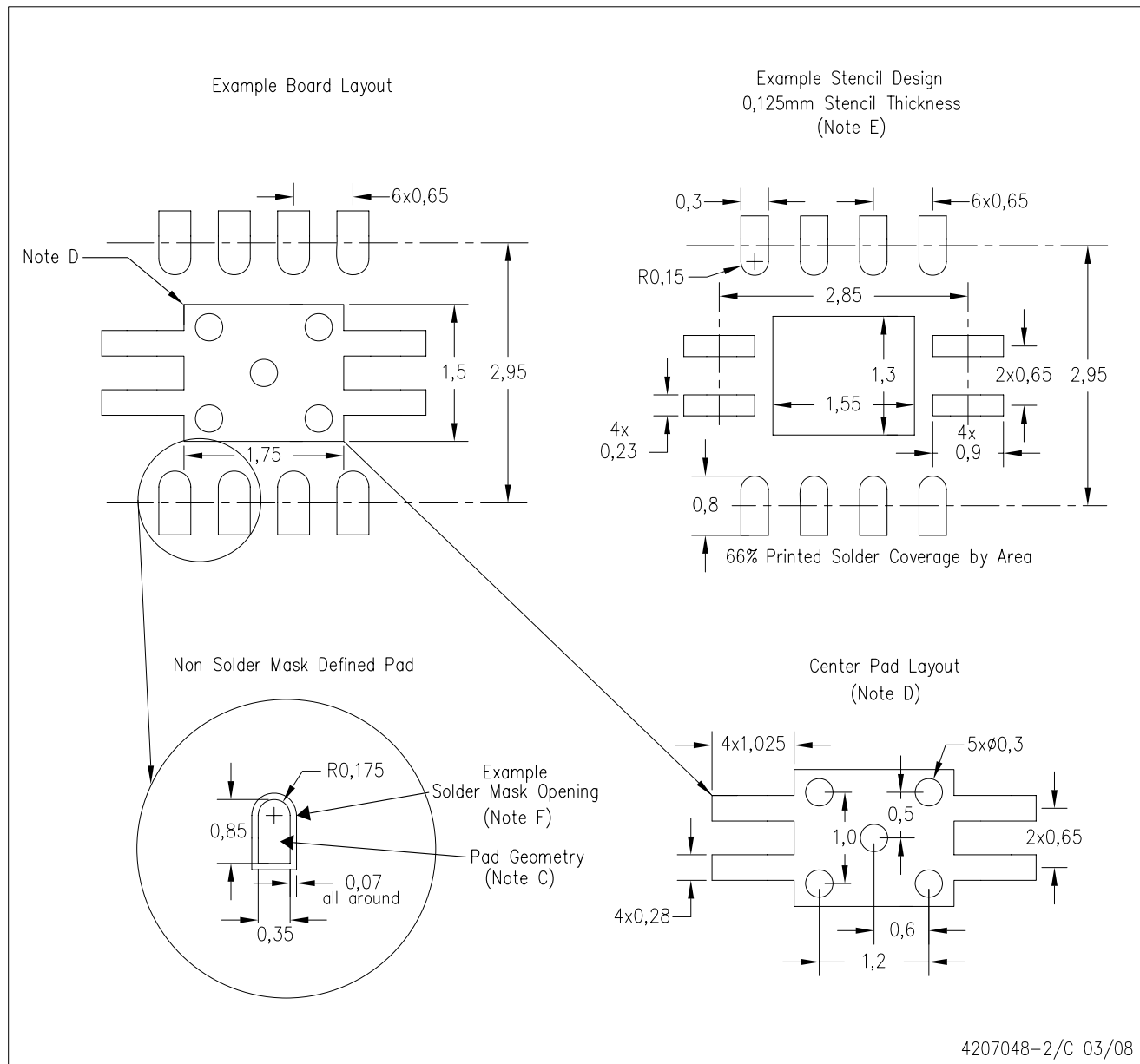


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRB (S-VSON-N8)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances.

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